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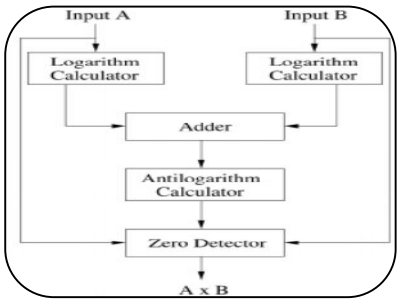
A STUDY ON LOGARITHM MULTIPLIER

Prerana Pundlik Autade
Research Scholar

ABSTRACT:



Real-time computing with low power is a basic need of various application areas such as digital signal processing, image processing, Internet of Things and neural networks. In real-time three-dimensional graphics systems, 86% of the data processing time is due to multiplication and division functions only. Logarithm multiplier hardware is a potential solution for efficient and fast multiplication operations. There is an absence of systematic literature on the entire development history and the procreations of logarithm multipliers in one place. This paper outlines the evolution and developments of Logarithm Multiplier Architecture Design and sheds light on potential research areas for further improvements. In this comprehensive study, researchers have included techniques used to improve the design of logarithm multipliers and have benefited from other reported multipliers that have been highlighted.

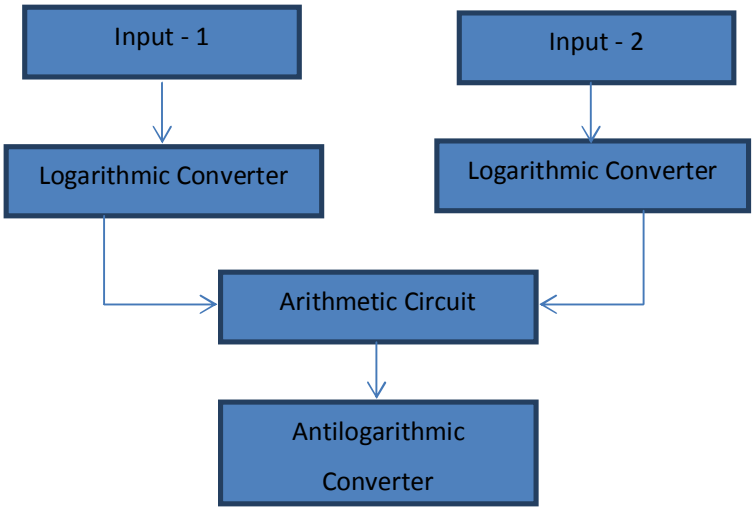
KEYWORDS: *Logarithm Multiplier, Architecture Design, Operand Decomposition.*

INTRODUCTION:

The rapid growth of integrated circuit technology has become a major impetus for real-time signal processing in the digital domain. Therefore, it is known that many arithmetic operations (such as multiplication, division, addition, subtraction, square root and power) are used in digital signal processing (DSP). In a three-dimensional graphics system, 86% of the data processing time is due to multiplication and division functions only. Multiplication is a widely used arithmetic operation in the field of DSP and image processing. It is known that the multiplier is a thirsty resource and its speed is always a limiting factor. Logarithmic number system (LNS) based multipliers offer greater advantages than fixed point (FXP) number systems and floating point (FLP) number system multipliers. The logarithmic multiplier converts the multiplication and division operation into addition and subtraction operations, respectively. The calculation of multiplication based on logarithm consists of three steps:

1. Logarithmic conversion of binary numbers for logarithmic representation,
2. Subsequent, arithmetic operations are performed in logarithmic domain and
3. Antilogarithmic conversion.

Figure 1.1 Computation of Arithmetic Based LNS



Logarithm Number System:

The binary number system has given issues of large area, delay and large power consumption in the operation of multiplication, division, root and power done in DSP application. But, the primary goal of DSP applications is to process operations with efficient hardware which cannot be fully filled due to the above mentioned problems of binary number system. LNS solves these problems and overcomes technical gaps. LNS provides a new approach to speed up multiplication and division with traditional weighted numbers.

Mathematicians have used logarithms to simplify mathematical operations such as multiplication, division, etc. because these operations can be done by addition and subtraction. LNS multipliers are more advantageous in terms of speed and accuracy than fixed point (FXP) multipliers and floating point (FLP) multipliers. The LNS multiplier supports two families of basic data-types: integer or fixed-point data and floating-point data. Fixed point multiplication is frequently used in general purpose digital processing applications due to its easy algorithm, fast implementation and clear understanding. However, the representation of a floating point is a suitable option where the decimal notation has the necessary criteria to represent a fractional number.

Following is the table which shows two binary numbers A and B of primary LNS arithmetic numbers.

Table 1.1 Logarithmic Arithmetic Operations

Binary Operations	Logarithmic Operations
Z = A X B	Log Z = Log A + Log B
Z = A / B	Log Z = Log A – Log B
Z = A + B	Log Z = Log A + Log_2 $(1+2^{(\text{Log B} - \text{Log A})})$
Z = A – B	Log Z = Log A + Log_2 $(1-2^{(\text{Log B} - \text{Log A})})$

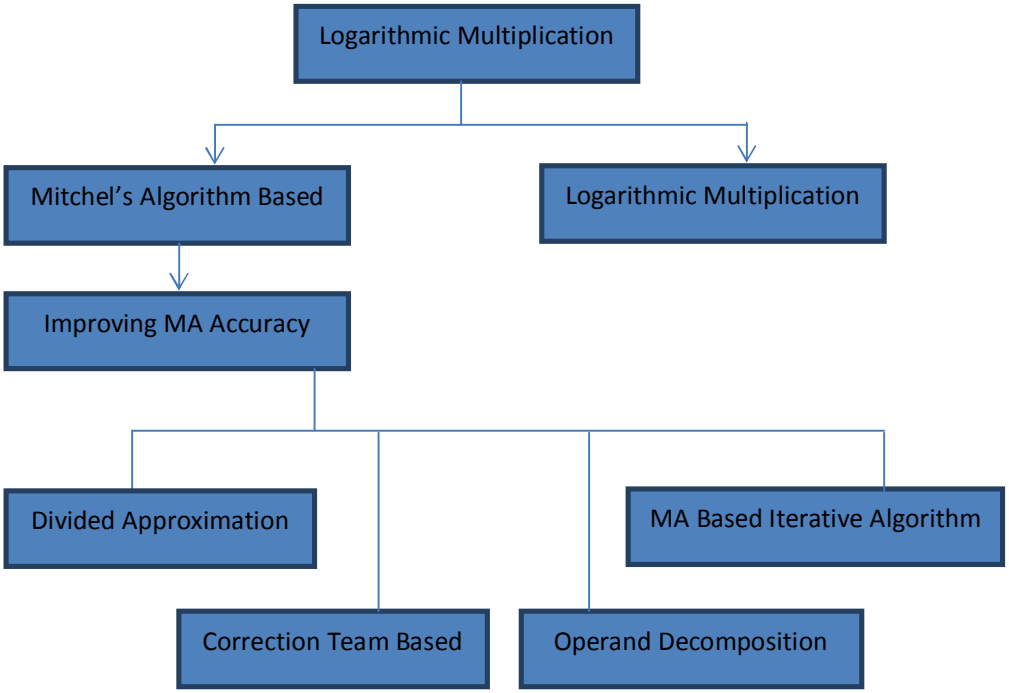
The general classification of logarithmic multiplication is shown in the figure below. LNS multipliers can be divided into two categories, (1) based on lookup tables and interpolation and (2) based on Mitchell's algorithms. Initial LNS based works were on launch plans. LNS multipliers based on interpolation schemes require read only memory (ROM) to store the required coefficients. The research work is applied to conversion to digit-repeating methods that save hardware costs but cost faster. However, 'shift-add-'d based schemes have been used to trade-off the right design in delay, area and accuracy. Mitchell's algorithm-based logarithm multiplication was divided into four subcategories.

1. Dividend Approximation
2. Correction term Based
3. Operand Decomposition
4. MA based Iterative Algorithm

In 1962, Mitchell reported an algorithm based on computer multiplication and simple addition and division operations of parts. In Mitchell's method, the average percentage error (APE) was 3.85% and the error percentage ranged from 0% to 11.11%. Hall's algorithm has been implemented but the shortcomings were accuracy in the cost of speed, power consumption and hardware complexity. In 1975, Swartzlander et al. Sine logarithm number systems and fast algorithms are suggested for basic arithmetic operations. In 1988, Taylor et al. the architectural design of the 20-bit logarithmic arithmetic processor is reported.

In 1991, U and Lewis noted the architectural design of a 30-bit logarithmic arithmetic processor. In 1999, Sangregari's correction algorithm was implemented which was easy and fast operation. In 2003, Abed and Seaford developed correction algorithms that indicate trade-offs in accuracy, speed, and complexity. In 2006, V. Mahalingam etc. have given operand decomposition (OD) as an independent approach to reduce errors. In 2008, Johansson et al. the approximate method is reported. In 2010, Funey et al reported. The approach of polynomial estimation is reported. Between 2010 and 2013, repetitive logarithmic estimates were presented based on correction terms with high-level parallelism. In 2017, DurgeshNandan et al have given revised operand decomposition (IOD) as an approach to reduce errors and applied previous logarithmic multiplication methods.

Figure 1.2 Logarithm Multiplication operations



RESULT AND DISCUSSION:

Error analysis can be performed with Mitchell's algorithm, Odymischel, iteration algorithm, and IOD-Mitchell multiplication with equal interval input vectors. The results are applied and applied with the same input patterns for unbiased error analysis, as shown in the table below.

Table 1.2 Comparison of Maximum Possible Error and Average Error Percentage

Method	AEP (%)			MPE (%)
	4-bit	8-bit	16-bit	
MA[4]	--	3.79	3.87	~14
OD-MA[26]	1.446	1.452	2.176	11.14
Iterative[27,28,29] (ECCs = 0)	---	8.917	9.427	26
Iterative[27,28,29] (ECCs = 1)	---	---	---	6.30
Iterative[27,28,29](ECCs = 1)	--	---	---	1.61
IOD-MA[30]	1.6281	1.681	2.071	11.14

Table 1.2 shows the 4-bit, 8-bit, and 16-bit multiplication widths and MPEs for Mitchell's algorithms, OD-Mitchell, iteration, and IOD-Mitchell multiplication. IOD-Mitchell multiplies 1.6281% APE for 4-bit, 1.681% for 8-bit and 2.176% for 16-bit, while OD-Mitchell multiplies 1.446% APE for 4-bit, 1.452% for 8-bit and 16- 2.176% for bits. The logarithmic multiplier offers 8.917% for 8-bits and 9.42% for 16-bits with repeat pipeline architecture. MPE is equal to 11.14% for OD-MA and IOD-MA, ~14% for Mitchell's algorithm and 26% for logarithmic multiplier with repeat pipeline architecture for zero error correction circuit.

The real world is full of applications of logarithm multipliers. Some of these applications are briefly discussed here. Approximate computing is an applicable technique for implementation in research areas such as image processing, video-signal processing and transmission. LNS are applied in video compression, especially in motion vectors. Multiplication circuits use a lot of area, time and power. Various LNS techniques can be used to overcome these problems. The concepts of digital image processing have been frequently used by various research fields such as astronomy, geography, medicine, etc. Due to the numerous applications of logarithm multipliers, it motivates researchers to take the lead in studying existing work and contributing to research efforts.

CONCLUSION:

In this paper we discuss LNS, how LNS is represented, logarithmic multiplier and systematic development in the field of its applications. This comprehensive study includes techniques used by researchers to improve the structure of logarithm multiplication. Based on this analysis, it was concluded that if accuracy is the main concern, the repetitive logarithmic multiplier is the best choice for designers. But, IOD based logarithm multiplication is the most efficient design in terms of area, speed, delay, accuracy. However, if the logarithm multiplier is applied by the logarithm converter and the antilogarithm converter with advanced correction circuits as suggested in the literature, it should become the most efficient design with the best performance. It is hoped that these improvements will lead to significant improvements in the field of digital signal processing systems and image processing.

REFERENCES:

1. AgrawalR.K. and Kittur H.M. ASIC basedlogarithmic multiplier using iterative pipelined architecture. *IEEE Conference on Information &Communication Technologies (ICT),* pp.362-366,2013.
2. Arnold M., Bailey T. and Cowles J. ErrorAnalysis of the Kmetz / Maenner Algorithm. *Journal of VLSI Signal Processing*. pp. 37-53, 2003.
3. BulicP., BabicZ. and Avramovic A. A simplepipelined logarithmic multiplier.*IEEEInternational Conference on Computer Design(ICCD)*, pp.235-240 (2010).
4. Cabello F., Leon J., Lana Y., and Arthur R.,Implementation of a Fixed-Point 2D GaussianFilter for Image Processing based on FPGA.*IEEE Signal Processing: Algorithms,Architectures, Arrangements, and Applications*,pp. 28-33, 2015.
5. DurgeshNandan, JitendraKanungo and AnuagMahajan. An efficient VLSI architecture design forlogarithmic multiplication by using the improved operand decomposition.*Integration, the VLSIJournal*, Vol. 58, pp. 134–141, *2017*.

6. DurgeshNandan, JitendraKanungo and AnuagMahajan. 65 Years Journey of Logarithm Multiplier. *International Journal of Pure and Applied Mathematics.* Vol-118, Issue-14, pp. 261-266. *2018*
7. Mahalingam V. and RangantathanN. ImprovingAccuracy in Mitchell's Logarithmic MultiplicationUsing Operand Decomposition, *IEEETransactions on Computers,* Vol. 55, No. 2, pp.1523-1535, *2006*.
8. Swartzlander E. and Alexopoulos A. The sign/logarithm number system. *IEEE Transaction on Computation*, Vol. C, pp. 1238–1242, 1975.
9. YuL. K., and LewisD. M. A 30-b IntegratedLogarithmic Number System Processor.*IEEEJournal of Solid State Circuits*, Vol. 26, No. 10,pp. 1433–1440, *1991*