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USING REVERSIBLE LOGIC GATES DESIGN OF 8 X 8 URDHVA TIRYAKBHYAM MULTIPLIER

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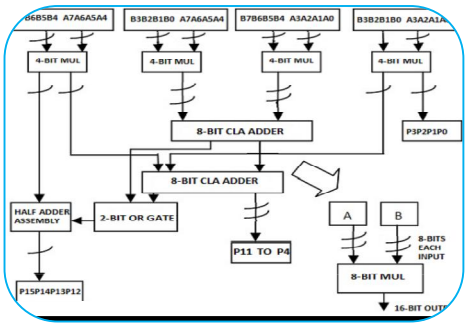
ABSTRACT



*Multiplication design is always a challenging task; Although many designs are proposed, the user needs a more optimized design. Vedic mathematics provides some algorithms that evaluate rapid results, both in mental calculations or in hardware design. Using reversible logic continuously reduces power dissipation. The reverse UrdhvaTiryakabhayam Vedic multiplier is a multiplier that is effective in terms of both speed and power. The improved design in this paper enhances the performance while maintaining the design efficiency without any degradation. The project is designed using 8 * 8 UT multiplier reversible logic gates and compares the results with a booth multiplier. Fast Fourier Transform (FFT) is the application of this multiplier to design filters and other applications of DSP such as imaging, software defined radio, wireless communications.*

KEYWORDS: *Reversible Logic Gates, UrdhvaTiryakbhyam Multiplier, Vedic Mathematics*

INTRODUCTION

High speed arithmetic operations are very important in many signal processing applications. The speed of a digital signal processor (DSP) is largely determined by the speed of its coefficients. In fact multipliers are the most important part of all digital signal processors; they are very important for carrying out many important tasks like Fast Fourier Transform and Convolution. Since the processor spends a lot of time multiplying, improving the multiplication speed can greatly improve the performance of the system. Multiplication can be applied using a number of algorithms such as Array, Booth, Carry Save and Wallace Tree algorithms. The computer time required by the array multiplier is less because partly the products are calculated separately in parallel. The delay associated with an array multiplier is the time it takes for the signal to be transmitted through the gates that make up the multiplied array. Adder arrangement is another way to improve multiplication speed. There are two methods for this: Carry Save Array (CSA) method and Wallace Tree method. In the CSA method, bits are processed one by one so that a carry signal is supplied to the adder at a slightly higher position.

The CSA method has its own limitations because the implementation time depends on the number of bits in the multiplier. In the Wallace Tree method, three bit signals are sent to a bit full adder and the sum is supplied to the next stage full adder of the same bit and the same number of carry output signal bits are given to the next stage full adder. And then the prepared carry is supplied to the next stage of complete addition at a slightly higher position. It is not easy to insert a circuit in this method.

The booth algorithm reduces the number of partial products. However, high speed multiplication and exponential operations require large booth arrays that require large partial sums and partial carry registers. Multiplication of two n-bit operands using a Radix-4 booth recording multiplier requires approximately n / (2m) clock cycles for at least a significant half of the final product, where m is the number of booth recorded er phases. Thus, a large diffusion delay is associated with this case. Improved Booth Encoded Wallace Tree Multiplier uses improved booth algorithms to reduce partial products, and faster connection is also made using Wallace Tree.

A binary multiplier is an electronic circuit used in digital electronics, such as a computer, to multiply two binary numbers. It is built using binary adders. A variety of computer arithmetic techniques can be used to apply digital multipliers. Many techniques involve calculating the set of partial products and then incorporating the partial products together. The process is similar to the method taught to elementary school children to multiply long on the base-10 integer, but has been modified here to apply for the base-2 (binary) number system. In the late 1970's, most minicomputers did not have multiplication instructions and so programmers used "multiplication routines" that change frequently and add partial results, often written using loop uninding. Mainframe computers had multiplication instructions, but they made similar shifts and added them as "multiplication routines."

Due to the large number of transistors available per chip due to the large aggregation, it was possible to add enough on a single chip to sum up the same partial products instead of reusing the same connection to handle each partial product at the same time. Because some common digital signal processing algorithms spend most of their time in multiplication, digital signal processor designers sacrifice a lot of chip area to multiply as fast as possible; Single-Cycle Multiply - Cumulative units usually use most of the chip area of the initial DSP.

Vedic Mathematics:

Vedic mathematics is one of the oldest methods used by the Aryans to calculate mathematics. It contains algorithms that can solve large arithmetic operations up to simple mind calculations. The advantage mentioned above is that the approach to Vedic mathematics is completely different and is considered very close to how the human mind works. The efforts made by Jagadguru Swami ShriBhartiKrishnatirtha Maharaja to introduce Vedic mathematics to the general public as well as to streamline Vedic algorithms in 16 categories or formulas must be acknowledged and appreciated. Vertical oblique is one such multiplication algorithm known for its efficiency in reducing the calculations involved. With the advancement of VLSI technology, there is an ever-increasing mitigation for portable and embedded digital signal processing (DSP) systems. DSP is ubiquitous in almost every branch of engineering. Fast addition and multiplication is the order of the day. Multiplication in CPU is the most basic and frequently used operation. Multiplication is the operation of counting one number by another.

Multiplication operations form the basis for other complex operations such as Convolution, Discrete Fourier Transform, Fast Fourier Transform, and so on. Therefore, DSP engineers are constantly looking for new algorithms and hardware to implement them. Vedic mathematics can be used correctly for multiplication here. The second important area that any DSP engineer is focused on is power dissipation, the first is speed. There is always a trade-off between power outage and speed of operation.

Reversible Logic Gates:

The reversible logic gate is a memory-less logic element that realizes the injectable logical function. Fredkin Gate, Tofoli Gate, Interaction Gate and Switch Gate are characteristic. Here, we examine the basic properties of reversible logic gates and circuits, which are required in the following chapters. First, their logical universality is discussed. Later, the construction method of almost waste-less reversible combinatorial logic circuit is explained. Reducing the total amount of waste signal is a major problem when designing a reversible logic circuit. Finally, the relationship between Fredkin Gate, reversible logic elements with 1-bit memory (RLEM) and reversible sequential machine (RSM) are studied. In particular, it has been shown that we can create completely waste-less circuits from Fredkin

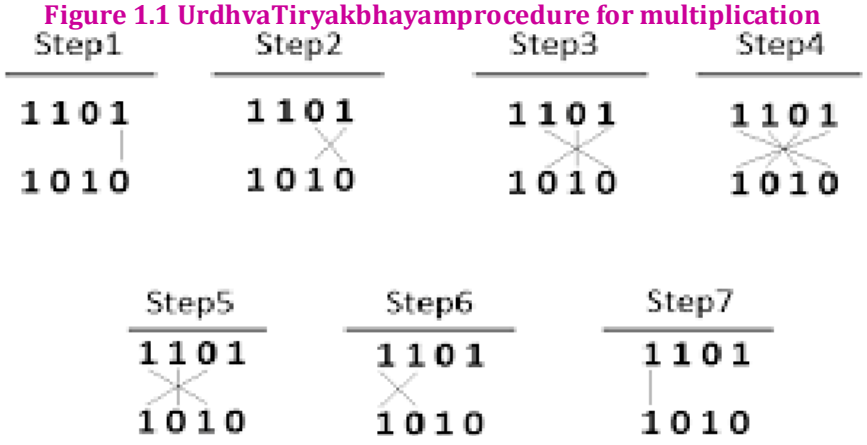
gates and delay components that mimic a given RSM.From the point of view of reversible circuit design, there are several parameters to determine the complexity and performance of a circuit.

Reducing these parameters is a major task involved in the design of reversible circuits. In this, a modified design of the reversible multiplier with respect to its rear parts is proposed. Multiplier circuits play an important role in computer operations using computers. Many arithmetic operations are performed on a computer's ALU using multipliers. The design and implementation of digital circuits has gained popularity for gaining access to future computer technology using reversible logic.

Urdhva Tiryakbhayam Multiplication Algorithm:

UrdhvaTiryakabhayam (UT) is a multiplier based on Vedic mathematical algorithms developed by ancient Indian Vedic mathematicians. The vertical oblique formula can be applied to all cases of multiplication e.g. Also binary, hex and decimal. It is based on the concept that all partial products can be manufactured and then these partial products are added simultaneously. Parallels and their summaries in the manufacture of semi-finished products are obtained using vertical slashes. Unlike other multipliers that increase the number of bits of multiplication and / or multiplier, the time delay in product calculation does not increase proportionally. Due to this fact the calculation time is independent of the clock frequency of the processor. Since processors that use low clock frequencies consume less energy, it is advantageous to use low frequency processors that use faster algorithms as mentioned above in terms of power factor. The advantage of a multiplier based on this formula is that as the number of bits increases, the gate delay and area increase slowly compared to other conventional multipliers.

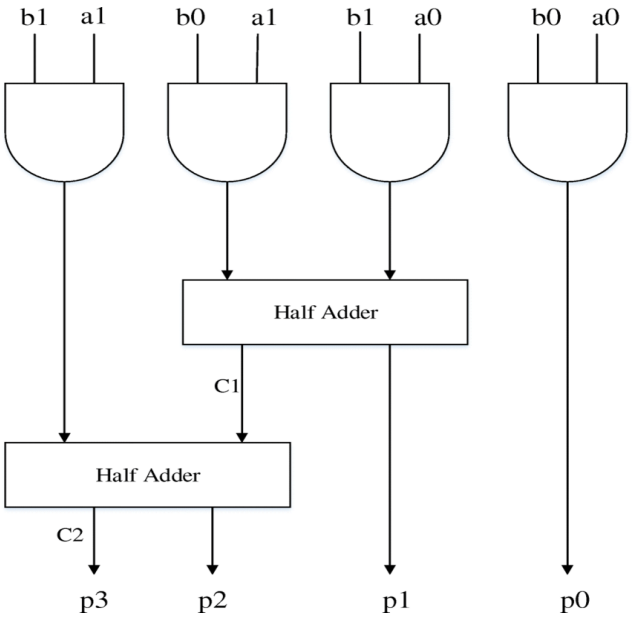
Figure 1.1 UrdhvaTiryakbhayamprocedure for multiplication



Optimization of the Urdhva Tiryakbhayam Multiplier:

Implementing traditional logic design of 2x2 vertical oblique multiplier using irreversible logic gates,the bits in the four expressions for the output are drawn from this figure and used for reversible execution. The circuit uses five Perez gates and one Feynman gate. The total quantum value of this structure is 21, the number of waste outputs is 11 and the number of continuous inputs is 4. The number of gates6. This design does not take into account the fan out. The overall performance of UT Multilayer is enhanced by optimizing each unit for quantum cost, waste output etc.

Figure 1.2 2 X 2 UrdhvaTiryakbhayam Multiplier



Booth Multiplier:

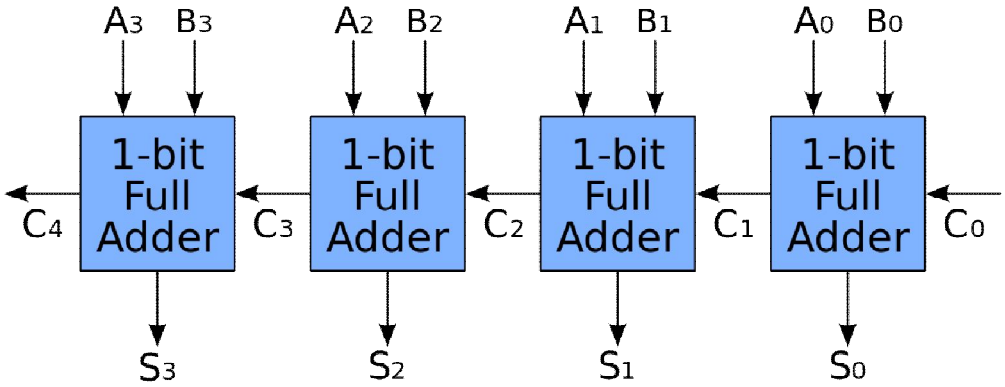
Booth's multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers into two complementary notations. The algorithm was invented by Andrew Donald Booth. Booth used a desk calculator that moved faster than a pair, and developed algorithms to increase speed. Booth's algorithm is of interest in the study of computer architecture. Booth's algorithm examines pairs adjacent to bits of the N-bit multiplier Y representing the compliance of the two signed, including the embedded bit below the least significant bit, $y_{-1} = 0$. For each bit y_{i-1}, i 0 to N-1 Running up to, y_i and y_{i-1} are considered bits. Where these two bits are equal, the product accumulator P remains unchanged. Where $y_i = 0$ and $y_{i-1} = 1$, the product is added 2' times to p; And where $y_i = 1$ and $y_{i-1} = 0$, the multiplication is subtracted from p times, the final value of P is the signed product.

Design of 8 X 8 UrdhvaTiryakbhayam Multiplier:

The inverse 8x8 vertical oblique multiplier design arises from the 2X2 multiplier. The block diagram of 8x8 Vedic multiplier is presented in the following figure. It consists of four 2X2 multipliers from which each takes four bits as input; Two bits from multiplication and two bits from multiplier. The bottom two bits of the output of the first 2X2 multiplier are stuck as the lowest two bits in the final result of the multiplication. Two zeros are connected with the top two bits and four bits are given to the ripple carry adder as input. The other four input bits for the Ripple Carry Adder are obtained from the second 2X2 multiplier.

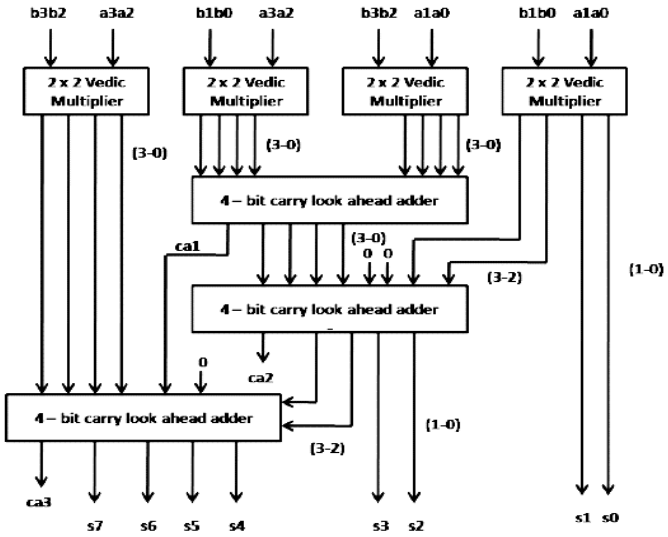
Similarly the outputs of the third and terminal 2X2 multipliers are given as inputs to the second four bit ripple carry adder. The outputs of these four bit ripple carry adders are 5 bits each which must be summarized. This is done by a five-bit ripple carry ad that generates a six-bit output. These six bits are in the upper bits of the final result. The structure shown in contains only HNG gates. The number of HNG gates is 4 if the ripple carrier is used in the second phase or five if the ripple carrier is used in the last phase of the 8x8 vertical oblique multiplier. The Ripple Carry Adder can be modified as follows. Since the input carry for the first complete adder is zero for any Ripple carry adder, this clearly means that the first adder is half the adder.

Figure 1.3 4 Bit Ripple Carry Adder



Since TRLIC is the sum of all design parameters, it is commendable that TRLIC has a minimum value. The proposed design of the reversible UT multiplier is compared with 11 different major multiplier designs in the literature in terms of quantum cost, number of waste outputs, number of gates, and number of continuous inputs. It also includes a comparison of our own previous design, and the optimization is clearly evident from the comparison table.

Figure 1.4 8 X 8 Vedic Multiplier



CONCLUSION:

In this project, the proposed 8 x 8 UT reversible Vedic multiplier is compared to the booth using Xilinx software under the specification of xc3s500e-4g320. The booth multiplier achieves a power of 42.2 NSC delay and 0.0029 watts, but the delay in the UT reversible Vedic multiplier is reduced to 25.1 NSC and power 0.0017 watts. Better performance than existing booth multipliers.

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